CLAIMS

1. A multilayer printed wiring board having conductor circuitry layers and interlaminar insulative resin layers deposited alternately one on another, the interlaminar insulative resin layers each having formed through them holes each filled with a plating layer to form a viahole, characterized by:

the surface of said plating layer exposed out of the hole for the viahole being formed substantially flat and lying in a substantially same level as the surface of the conductor circuit layer disposed in the interlaminar insulative resin layer in which the plating layer also lies; and

the thickness of said conductor circuitry layer being less than a half of the viahole diameter.

2. The multilayer printed wiring board as set forth in Claim 1, wherein the inner wall of the hole is roughened.

3. The multilayer printed wiring board as set forth in Claim 1 ~~or 2~~, wherein the plating layer surface and conductor circuit surface exposed out of the hole for the viahole are roughened.

4. The multilayer printed wiring board as set forth in ~~any one of~~ Claims 1 ~~to 3~~, wherein the surfaces of the inner conductor circuits connected to each other by the viahole are roughened.

5. The multilayer printed wiring board as set forth in ~~any one of~~ Claims 1 ~~to 4~~, wherein a further viahole is formed on the viahole.

6. The multilayer printed wiring board as set forth in ~~any of~~ Claims 1 ~~to 5~~, wherein the interlaminar insulative resin layer in which the viaholes are formed is made of a thermoplastic resin or a composite of thermoplastic and thermosetting resins.

7. The multilayer printed wiring board as set in ~~any of~~ Claims 1 ~~to 6~~, wherein the ratio between the viahole diameter and interlaminar insulative resin layer is within a range of

1 to 4.

8. The multilayer printed wiring board as set forth in ~~any of~~ Claims 1 ~~to 7~~, wherein the conductor circuitry layer has a thickness less than 25 μm.

9. A multilayer printed wiring board having conductor circuitry layers and interlaminar insulative resin layers deposited alternately one on another, the interlaminar insulative resin layers each having formed through them holes each filled with a plating layer to form a viahole, characterized in that the thickness of said conductor circuitry layer is less than a half of the viahole diameter and less than 25 μm.

10. The multilayer printed wiring board as set forth in Claim 9, wherein the inner wall of the hole is roughened.

11. The multilayer printed wiring board as set forth in Claim 9 ~~or 10~~, wherein a depression is formed on the central surface portion of the plating layer surface exposed out of the hole for the viahole.

12. The multilayer printed wiring board as set forth in ~~any one of~~ Claims 9 ~~to 11~~, wherein the plating layer surface and conductor circuit surface exposed out of the hole for the viahole are roughened.

13. The multilayer printed wiring board as set forth in ~~any one of~~ Claims 9 ~~to 12~~, wherein the surfaces of the inner conductor circuits connected to each other by the viahole are roughened.

14. The multilayer printed wiring board as set forth in ~~any one of~~ Claims 9 ~~to 13~~, wherein a further viahole is formed on the viahole.

15. The multilayer printed wiring board as set forth in ~~any of~~ Claims 9 ~~to 14~~, wherein the interlaminar insulative resin layer in which the viaholes are formed is made of a thermoplastic resin or a composite of thermoplastic and thermosetting resins.

16. The multilayer printed wiring board as set in ~~any of~~ Claims 9 ~~to 15~~, wherein the ratio between the viahole diameter and interlaminar insulative resin layer is within a range of 1 to 4.

17. A multilayer printed wiring board having conductor circuitry layers and interlaminar insulative resin layers deposited alternately one on another, the interlaminar insulative resin layers each having formed through then holes each filled with a plating layer to form a viahole, characterized by:

said hole having an inner wall thereof roughened;

said roughened inner wall being covered with a roughened electroless plating layer; and

an inner space of said hole defined by the electroless plating layer and filled with an electroplating layer.

18. The multilayer printed wiring board as set forth in Claim 17, wherein depressions are formed in the central surface portion of the plating layer surface exposed out of the hole for the viahole.

19. The multilayer printed wiring board as set forth in ~~any~~ Claim 17 ~~or 18~~, wherein the plating layer surface and conductor circuit surface exposed out of the hole for the viahole are roughened.

20. The multilayer printed wiring board as set forth in ~~any one of~~ Claims 17 ~~to 19~~, wherein the surfaces of the inner conductor circuits connected to each other by the viahole are roughened.

21. The multilayer printed wiring board as set forth in ~~any one of~~ Claims 17 ~~to 20~~, wherein a further viahole is formed on the viahole.

22. The multilayer printed wiring board as set forth in ~~any of~~ Claims 17 ~~to 21~~, wherein the interlaminar insulative resin layer in which the viaholes are formed is made of a thermoplastic

resin or a composite of thermoplastic and thermosetting resins.

23. The multilayer printed wiring board as set in ~~any of~~ Claims 17 ~~to 22~~, wherein the ratio between the viahole diameter and interlaminar insulative resin layer is within a range of 1 to 4.

24. The multilayer printed wiring board as set forth in ~~any of~~ Claims 17 ~~to 23~~, wherein the conductor circuitry layer has a thickness less than 25 μm.

25. A multilayer printed wiring board having conductor circuitry layers and interlaminar insulative resin layers deposited alternately one on another, the interlaminar insulative resin layers each having formed through them holes each filled with a plating layer to form a viahole, characterized by:

said interlaminar insulative resin layer being formed from a composite of fluororesin and heat-resistant thermoplastic resin, composite of fluororesin and thermosetting resin, or a composite of thermosetting resin and heat-resistant thermoplastic resin.

26. The multilayer printed wiring board as set forth in Claim 25, wherein the interlaminar insulative resin layer is made of a composite of fluororesin fiber cloth and thermosetting resin impregnated in the voids in the cloth.

27. The multilayer printed wiring board as set forth in Claim 25 ~~or 26~~, wherein the inner wall of the hole is roughened.

28. The multilayer printed wiring board as set forth in ~~any of~~ Claims 25 ~~to 27~~, wherein depressions are formed in the central surface portion of the plating layer surface exposed out of the hole for the viahole.

29. The multilayer printed wiring board as set forth in ~~any one of~~ Claims 25 ~~to 28~~, wherein the plating layer surface and conductor circuit surface exposed out of the hole for the viahole

are roughened.

30. The multilayer printed wiring board as set forth in ~~any one of~~ Claims 25 ~~to 29~~, wherein the surfaces of the inner conductor circuits connected to each other by the viahole are roughened.

31. The multilayer printed wiring board as set forth in ~~any one of~~ Claims 25 ~~to 30~~, wherein a further viahole is formed on the viahole.

32. The multilayer printed wiring board as set in ~~any of~~ Claims 25 ~~to 31~~, wherein the ratio between the viahole diameter and interlaminar insulative resin layer is within a range of 1 to 4.

33. The multilayer printed wiring board as set forth in ~~any of~~ Claims 25 ~~to 32~~, wherein the conductor circuitry layer has a thickness less than 25 μm.

34. (canceled)

are roughened.

30. The multilayer printed wiring board as set forth in any one of Claims 25 to 29, wherein the surfaces of the inner conductor circuits connected to each other by the viahole are roughened.

31. The multilayer printed wiring board as set forth in any one of Claims 25 to 30, wherein a further viahole is formed on the viahole.

32. The multilayer printed wiring board as set in any of Claims 25 to 31, wherein the ratio between the viahole diameter and interlaminar insulative resin layer is within a range of 1 to 4.

33. The multilayer printed wiring board as set forth in any of Claims 25 to 32, wherein the conductor circuitry layer has a thickness less than 25 μm.

34. A multilayer printed wiring board having conductor circuitry layers and interlaminar insulative resin layers deposited alternately one on another, the interlaminar insulative resin layers each having formed through them holes each filled with a plating layer to form a viahole, characterized by a solder bump being formed on the viahole.